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3. (Three times Amended) The method according to claim 30, wherein the metal layer comprises titanium.

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4. (Three times Amended) The method according to claim 30, wherein the supplemental silicon layer is poly-silicon formed by a chemical vapor deposition technique.

5. (Three times Amended) The method according to claim 30, wherein the supplemental silicon layer is amorphous silicon formed by a sputtering technique.

6. (Three times Amended) The method according to claim 30, further comprising:
selectively removing non-reacted silicon from the second-reacted silicide region
after the second rapid thermal annealing.

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24. (Twice Amended) A method for fabricating a semiconductor device, comprising:

- providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate;
- forming a metal layer on the silicon region of the semiconductor substrate;
- performing a first rapid thermal annealing on the semiconductor substrate to form first-reacted silicide regions;
- forming a supplemental silicon layer on the first-reacted silicide regions;

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doping an impurity into the supplemental silicon layer; and
performing a second rapid thermal annealing to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

E2

the semiconductor device including a p-channel MOS transistor having p-type source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping a p-type impurity into the supplemental silicon layer that is formed over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is formed over the n-channel MOS transistor.

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25. (Amended) The method according to claim 24, wherein the metal layer comprises cobalt.

26. (Amended) The method according to claim 24, wherein the metal layer comprises titanium.

27. (Amended) The method according to claim 24, wherein the supplemental silicon layer is poly-silicon formed by a chemical vapor deposition technique.

28. (Amended) The method according to claim 24, wherein the supplemental silicon layer is amorphous silicon formed by a sputtering technique.

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29. (Amended) The method according to claim 24, further comprising:
selectively removing non-reacted silicon from the second-reacted silicide regions
after the second rapid thermal annealing.

Please add claim 30 as follows:

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--30. A method for fabricating a semiconductor device comprising:
providing a silicon substrate;
providing a buried oxide layer on the silicon substrate;
providing a field oxide layer and a silicon on insulator layer on the buried oxide
layer;
providing a gate oxide layer on the silicon on insulator layer;
providing a poly-silicon gate layer on the gate oxide layer;
providing a gate side wall layer on the silicon on insulator layer to surround the
poly-silicon gate layer and the gate oxide layer;
providing a material to be silicided on a surface of the semiconductor device
including the poly-silicon gate layer, the gate side wall layer, the silicon on insulator
layer and the field oxide layer;
performing a first rapid thermal annealing process to form first-reacted silicide
regions in the poly-silicon gate layer and in source/drain active areas of the silicon on
insulator layer;
removing non-reacted material from the first-reacted silicide regions;
providing a supplemental silicon layer over the surface of the semiconductor

device after the non-reacted material is removed;

doping the supplemental silicon layer; and

performing a second rapid thermal annealing process to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

the supplemental silicon layer preventing the poly-silicon gate layer and the silicon on insulator layer from being completely silicided,

the semiconductor device including a p-channel MOS transistor having p-type source and drain regions, and including an n-channel MOS transistor having n-type source and drain regions,

said doping comprising doping a p-type impurity into the supplemental silicon layer that is provided over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is provided over the n-channel MOS transistor.--